Remarks

The Office Action dated 22 August 2002 has been received and reviewed. Claims 23, 27, and 31-32 have been amended. The pending claims are claims 23-49. Reconsideration and withdrawal of the rejections are respectfully requested.

Claim Amendments

Claim 23 was amended to recite a chemical vapor deposited barrier layer over at least a portion of the surface, wherein the barrier layer is formed of a platinum(x):ruthenium(1-x) alloy, where x is in the range of about 0.60 to about 0.995, and further wherein the barrier layer is substantially free of carbon. Support for this amendment may be found in the Specification, e.g., beginning at page 11, line 6 as amended herein.

Claim 27 was amended to recite that the second electrode includes a chemical vapor deposited barrier layer of platinum(x):ruthenium(1-x) alloy, and further wherein the barrier layer is substantially free of carbon. Support for this amendment may be found in the Specification, e.g., beginning at page 11, line 6 as amended herein.

Claim 31 was amended to correct a typographical error.

Claim 32 was amended to recite that the capacitor includes at least one electrode including a chemical vapor deposited barrier layer formed of platinum(x):ruthenium(1-x) alloy, wherein the barrier layer is substantially free of carbon. Support for this amendment may be found in the Specification, e.g., beginning at page 11, line 6 as amended herein.

Specification Amendment

The paragraph beginning at page 11, line 6 was amended as described herein to include language imported from co-pending application entitled "Method for Providing Low Carbon/Oxygen Conductive Layers" having U.S. Serial No. 09/146,297, filed September 3, 1998, and issued as U.S. Patent No. 6,284,655 B1. Such application was incorporated by reference in the present application as filed (see, e.g., page 17, line 23). Support for this

amendment may be found at various locations within the disclosure of the '655 patent, e.g., in the Abstract.

Claim Objections

The Examiner objected to claims 27 and 31 because of informalities. In response, Applicant has amended claims 27 and 31 to correct typographical errors.

The 35 U.S.C. § 102 Rejections

The Examiner rejected claims 23-24 and 26-48 under 35 U.S.C. § 102(e) as being anticipated by Dornfest et al. Applicant traverses this rejection.

However, to move this case towards issuance, Applicant has amended independent claims 23, 27, and 32. Applicant submits that claims 23-24 and 26-48 are not anticipated by Dornfest et al. for at least the following reasons.

For a claim to be anticipated under 35 U.S.C. § 102(e), each and every element of the claim must be found in a single prior art reference. *See* M.P.E.P. § 2131.

Applicant submits that claims 23-24 and 26-48 are patentable because Dornfest et al. does not teach each and every element of such claims. For example, independent claims 23, 27, and 32 each recite a chemical vapor deposited barrier layer that is substantially free of carbon. In contrast to these claims, Dornfest et al. teaches a top interface layer 50 that may include a combination of platinum and ruthenium, where the layer 50 may be formed by either PVD or CVD. Dornfest et al. does not teach a chemical vapor deposited barrier layer that is substantially free of carbon, as is recited by claims 23, 27, and 32. Because Dornfest et al. does not teach each and every element of claims 23, 27, and 32, Dornfest et al. cannot anticipate such claims.

Further, for example, claim 37 recites an interconnect that includes a barrier layer formed of platinum(x):ruthenium(1-x) alloy. In contrast to claim 37, Dornfest et al. teaches various capacitor structures. The embodiment of Dornfest et al. relied upon by the Examiner to reject claim 37 (i.e., FIG. 2) includes a capacitor 32a including an upper electrode 36, a lower electrode 38, and a high k dielectric or HDC layer 40 separating the upper and lower electrodes. *See*

Dornfest et al., column 4, lines 26-29. In other words, the alleged interconnect 38 is actually a lower electrode of capacitor 32a.

With regard to claims 24, 26, 28-31, 33-36, and 38-48, each of which depend, either directly or ultimately, from one of independent claims 23, 27, 32, or 37, claims 24, 26, 28-31, 33-36, and 38-48 are not anticipated by Dornfest et al. for the same reasons as presented above for claims 23, 27, 32, and 37. In addition, claims 24, 26, 28-31, 33-36, and 38-48 each recite additional elements that further support patentability.

For at least the above reasons, Applicant submits that claims 23-24 and 26-48 are not anticipated by Dornfest et al. Reconsideration and withdrawal of this rejection are, therefore, respectfully requested.

The Examiner also rejected claims 23, 26-27, 32, 37, 40-41, and 44-45 under 35 U.S.C. § 102(e) as being anticipated by Wolters et al.

Applicant traverses this rejection and submits that claims 23, 26-27, 32, 37, 40-41, and 44-45 are not anticipated by Wolters et al. For example, independent claims 23, 27, and 32 each recite a chemical vapor deposited barrier layer that is substantially free of carbon. Wolters et al., on the other hand, teaches a capacitor having a lower electrode 11 that includes ruthenium layer 110 with approximately 25% platinum, and a platinum layer 111 that includes approximately 15-20% ruthenium. *See* Wolters et al., column 7, lines 5-8. These layers are formed by sputtering a ruthenium layer followed by sputtering a platinum layer on the ruthenium layer. *See id.* at column 6, line 66 through column 7, line 3. The layers are then baked to produce the ruthenium/platinum and platinum/ruthenium layers 110 and 111 respectively. Wolters et al. does not teach a chemical vapor deposited barrier layer that is substantially free of carbon as recited by claims 23, 27, and 32; therefore, Wolters et al. cannot anticipate such claims.

Further, for example, claim 37 recites an interconnect that includes a barrier layer formed of platinum(x):ruthenium(1-x) alloy. In contrast to claim 37, the embodiment of Wolters et al. relied upon by the Examiner to reject claim 37 (i.e., FIG. 6) is a capacitor as described above. In other words, Wolters et al. does not teach an interconnect structure as claimed in claim 37.

With regard to claims 26, 40-41, and 44-45, each of which depend, either directly or ultimately, from one of independent claims 23, 27, 32, or 37, claims 26, 40-41, and 44-45 are not anticipated by Wolters et al. for the same reasons as presented above for claims 23, 27, 32, and 37. In addition, claims 26, 40-41, and 44-45 each recite additional elements that further support patentability.

For at least the above reasons, Applicant submits that claims 23, 26-27, 32, 37, 40-41, and 44-45 are not anticipated by Wolters et al. Reconsideration and withdrawal of this rejection are, therefore, respectfully requested.

The Examiner further rejected claims 23, 26-27, 32, and 37 under 35 U.S.C. § 102(e) as being anticipated by Kawakubo et al.

Applicant traverses this rejection and submits that claims 23, 26-27, 32, and 37 are patentable because Kawakubo et al. does not teach each and every element of such claims. For example, each of claims 23, 26-27, and 32 recite a chemical vapor deposited barrier layer that is substantially free of carbon. In contrast to these claims, the embodiment of Kawakubo et al. relied upon by the Examiner (i.e., FIG. 5E) teaches a semiconductor memory device including a bottom electrode 13 made of a platinum/ruthenium alloy deposited by DC sputtering. *See* Kawakubo et al., column 9, lines 32-34. In other words, Kawakubo et al. does not teach each and every element of claims 23, 26-27, 32, and 37.

Further, claim 37 recites an interconnect that includes a barrier layer formed of platinum(x):ruthenium(1-x) alloy. In contrast to claim 37, the embodiment of Kawakubo et al. relied upon by the Examiner (i.e., FIG. 5E) teaches a semiconductor memory device including a bottom electrode 13 made of a platinum/ruthenium alloy deposited by DC sputtering. In other words, Kawakubo et al. does not teach an interconnect structure as claimed in claim 37.

For at least the above reasons, Applicant submits that claims 23, 26-27, 32, and 37 are not anticipated by Kawakubo et al. Reconsideration and withdrawal of this rejection are, therefore, respectfully requested.

The 35 U.S.C. § 103(a) Rejection

The Examiner rejected claims 25 and 49 under 35 U.S.C. § 103(a) as being unpatentable over Dornfest et al. or Kawakubo et al. Applicant traverse this rejection and submits that claims 25 and 49 are patentable over both Dornfest et al. and Kawakubo et al. for at least the following reasons.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art references must teach or suggest all the claim limitations. *See* M.P.E.P. § 2143.

Claims 25 and 49 are not *prima facie* obvious because neither Dornfest et al. nor Kawakubo et al. teach all of the elements of such claims. For example, claim 25, which ultimately depends from claim 23, includes all of the elements of claim 23. As stated above for the 35 U.S.C. § 102(e) rejection of claim 23, Dornfest et al. does not teach all of the elements of claim 23 (e.g., a chemical vapor deposited barrier layer that is substantially free of carbon). Further, as also stated above, Kawakubo et al. does not teach every element of claim 23. Therefore, the combination of Dornfest et al. and Kawakubo et al. fail to render claim 25 *prima facie* obvious.

Further, for example, claim 49 ultimately depends from claim 37 and, therefore, includes all of the elements of claim 37. As stated above, neither Dornfest et al. nor Kawakubo et al. teaches all of the elements of claim 37 (e.g., an interconnect including a barrier layer). Therefore, the combination of Dornfest et al. and Kawakubo et al. fail to render claim 49 *prima facie* obvious.

For at least the above reasons, Applicant submits that claims 25 and 49 are not *prima facie* obvious in view of the cited references. Reconsideration and withdrawal of this rejection are, therefore, respectfully requested.

Summary

It is respectfully submitted that the pending claims are in condition for allowance and notification to that effect is respectfully requested. The Examiner is invited to contact Applicant's Representatives, at the below-listed telephone number, if it is believed that prosecution of this application may be assisted thereby.

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CERTIFICATE UNDER 37 C.F.R. § 1.8:
The undersigned hereby certifies that this paper is being transmitted by facsimile in accordance with 37 C.F.R. § 1.6(d) to the Patent and Trademark Office, addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on this 21st day of January, 2003 at 3:40 pm (Central Time).

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APPENDIX A - SPECIFICATION/CLAIM AMENDMENTS INCLUDING NOTATIONS TO INDICATE CHANGES MADE
Serial No.: 09/942,200
Docket No.: 150.00640102

Amendments to the following are indicated by underlining what has been added and bracketing what has been deleted.

In the Specification

The paragraph beginning at page 11, line 6, has been amended as follows:

--Methods of forming the co-deposited platinum:ruthenium alloy layer 14 are described in co-pending patent application entitled "Method for Producing Low Carbon/Oxygen Conductive Layers" having U.S. Serial No. 09/146,297, filed September 3, 1998, and issued as U.S. Patent No. 6,284,655 B1. For example, one such method includes forming a substantially carbon- and oxygen-free conductive layer in an oxidizing atmosphere in the presence of an organometallic catalyst using a chemical vapor deposition process. One skilled in the art will recognize that these methods and various other methods may be used to form the platinum:ruthenium alloy layer 14 according to the present invention.--

In the Claims

For convenience, all pending claims are shown below.

23. **(Once Amended)** A semiconductor device structure, the structure comprising:
a substrate assembly including a surface; and
a chemical vapor deposited barrier layer over at least a portion of the surface, wherein the barrier layer is formed of a platinum(x):ruthenium(1-x) alloy, where x is in the range of about 0.60 to about 0.995, and further wherein the barrier layer is substantially free of carbon.

24. The structure of claim 23, wherein x is in the range of about 0.90 to about 0.98.

25. The structure of claim 24, wherein x is about 0.95.

26. The structure of claim 23, wherein the portion of the surface is a silicon containing surface.

27. **(Once Amended)** A capacitor structure comprising:

a first electrode;

a dielectric material on at least a portion of the first electrode; and

a second electrode on the dielectric material, wherein at least one of the first electrode and second electrode comprises a chemical vapor deposited barrier layer of platinum(x):ruthenium(1-x) alloy, and further wherein the barrier layer is substantially free of carbon.

28. The structure of claim 27, wherein x is in the range of about 0.60 to about 0.995.

29. The structure of claim 28, wherein x is in the range of about 0.90 to about 0.98.

30. The structure of claim 27, wherein at least one of the first electrode and second electrode comprises the barrier layer of platinum(x):ruthenium(1-x) alloy and one or more additional conductive layers.

31. **(Once Amended)** The structure of claim 30, wherein the one or more additional conductive layers are formed from materials selected from [materials selected from] the group of metals and metal alloys; metal and metal alloy oxides; metal nitrides; and metal silicides.

32. **(Once Amended)** A memory cell structure comprising:

a substrate assembly including at least one active device; and

a capacitor formed relative to the at least one active device, the capacitor comprising at least one electrode including a chemical vapor deposited barrier layer formed of platinum(x):ruthenium(1-x) alloy, wherein the barrier layer is substantially free of carbon.

33. The structure of claim 32, wherein the capacitor includes:

a first electrode formed relative to a silicon containing region of the at least one active device;

a dielectric material on at least a portion of the first electrode; and

a second electrode on the dielectric material, wherein the first electrode comprises the barrier layer formed of platinum(x):ruthenium(1-x) alloy.

34. The structure of claim 33, wherein the first electrode comprising the barrier layer formed of platinum(x):ruthenium(1-x) alloy includes one or more additional conductive layers.

35. The structure of claim 33, wherein x is in the range of about 0.60 to about 0.995.

36. The structure of claim 35, wherein x is in the range of about 0.90 to about 0.98.

37. An integrated circuit structure comprising:

a substrate assembly including at least one active device; and

an interconnect formed relative to the at least one active device, the interconnect including a barrier layer formed of platinum(x):ruthenium(1-x) alloy.

38. The structure of claim 37, wherein x is in the range of about 0.60 to about 0.995.

39. The structure of claim 38, wherein x is in the range of about 0.90 to about 0.98.

40. The structure of claim 23, wherein the barrier layer comprises a chemical vapor deposited barrier layer.

41. The structure of claim 23, wherein the at least a portion of the surface defines a small high aspect ratio opening.

42. The structure of claim 23, wherein a thickness of the barrier layer is in a range of about 10 Å to about 10,000 Å.

43. The structure of claim 42, wherein the thickness of the barrier layer is in a range of about 100 Å to about 500 Å.

44. The structure of claim 23, wherein the substrate assembly comprises at least one active device.

45. The structure of claim 37, wherein the barrier layer comprises a chemical vapor deposited barrier layer.

46. The structure of claim 37, wherein the substrate assembly comprises a small high aspect ratio opening, and further wherein the interconnect is formed in the small high aspect ratio opening relative to the at least one active device.

47. The structure of claim 37, wherein a thickness of the barrier layer is in a range of about 10 Å to about 10,000 Å.

48. The structure of claim 47, wherein the thickness of the barrier layer is in a range of about 100 Å to about 500 Å.

49. The structure of claim 39, wherein x is about 0.95.